Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A computer implemented method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining whether the initiator or the interconnect is to be responsible for ordering packet-format responses to packet-format requests issued by said initiator;

determining whether to define a maximum number of packet format requests which are permitted to be outstanding at the same time;

defining whether a delay stage is required in said initiator; and

processing results of the defining steps and the determining step to produce a description of the integrated circuit.

~~representing results of the defining and determining steps as parameters stored in a computer file.~~

Claim 2 (previously presented): A method as claimed in claim 1, wherein said number of requests which are permitted to be outstanding are defined when the interconnect is responsible for ordering.

Claim 3 (currently amended): A computer implemented method for designing a target in an integrated circuit, said target being connected to an interconnect and arranged to generate packet format responses to packet format requests, the method comprising the steps of:

defining whether the target or the interconnect is responsible for ordering responses;

determining whether to define a maximum number of possible outstanding requests which can be supported by said target;

defining whether a delay stage is required in said target; and

producing a description of the integrated circuit based on the defining steps and the determining step.

~~representing results of the defining and determining steps as parameters stored in a computer file.~~

Claim 4 (previously presented): A method as claimed in claim 3, wherein said step of defining the maximum number of possible outstanding requests is performed when the interconnect is responsible for ordering the responses.

Claim 5 (currently amended): A computer implemented method for designing an interconnect having routing resources, said interconnect arranged to allow initiators to send packet-format requests to targets, said method comprising the steps of defining:

the number of routing resources between the initiator and the target;

the arbitration method for arbitrating between requests; and

the association between the routing resources and the targets; and

processing results of the defining steps and the determining step to produce a description of an integrated circuit comprising the interconnect.

~~representing the defined number of routing resources, defined arbitration method, and defined association as parameters stored in a computer file.~~

Claim 6 (original): A method as claimed in claim 5, wherein said method further comprises the step of determining if a delay is required after arbitration.

Claim 7 (currently amended): A computer implemented method for designing an interconnect having routing resources, said interconnect arranged to allow targets to send packet-format responses to initiators in response to packet-format requests from initiators, said method comprising the steps of defining:

the number of routing resources between the target and the initiator;

the arbitration method for arbitration between responses;

the association between the routing resources and the initiator; and

producing a description of the integrated circuit based on parameters generated in the defining steps and the determining step.

~~representing the defined number of routing resources, defined arbitration method, and defined association as parameters stored in a computer file.~~

Claim 8 (original): A method as claimed in claim 7, wherein said method further comprises the step of determining if a delay is required after arbitration.

Claim 9 (currently amended): A computer implemented method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model; and

producing a description of the integrated circuit using the selected one of the plurality of arbitration methods.

~~representing the selected arbitration method as a parameter stored in a computer file.~~

Claim 10 (currently amended): A computer implemented method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model, wherein the method further comprises selecting whether a delay is to be provided after arbitration has been performed; and

producing a description of the integrated circuit using the selected one of the arbitration methods and results of the selecting of whether a delay is to be provided after arbitration has been performed.

~~representing the selected arbitration method as a parameter stored in a computer file; and~~

~~representing whether a delay is to be provided as a parameter in the computer file..~~

Claim 11 (currently amended): A computer implemented method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model; and

producing a description of the integrated circuit using output of the selected one of the arbitration methods.

~~representing the selected arbitration method as a parameter stored in a computer file.~~

Claim 12 (currently amended): A computer implemented method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model, wherein the method further comprises selecting if a delay is to be provided after arbitration has been performed; and

producing a description of the integrated circuit using the selected one of the arbitration methods and results of the selecting of whether a delay is to be provided after arbitration has been performed.

~~representing the selected arbitration method as a parameter stored in a computer file; and~~

~~representing whether a delay is to be provided as a parameter in the computer file.~~

Claim 13 (currently amended): A model of an initiator implemented in a computer to be used in designing an integrated circuit in which an initiator is arranged to send packet-format requests to one or more targets via an interconnect, said model embodied as a plurality of parameters stored in a computer file, said model comprising:

an address decode stage running on the computer for identifying the target for which a given message is intended; and

a dependency stage running on the computer for determining the allowability of a request, the operation of said dependency stage being selectable, said dependency stage being such that the model supports an arrangement where the initiator or the interconnect is responsible for maintaining the order of packet-format responses from a target to the requests.

Claim 14 (original): A model as claimed in claim 13, wherein a retime stage is provided in said model, the retime stage arranged to provide a delay or no delay.

Claim 15 (previously presented): A model as claimed in claim 13, wherein an access queue is provided for storing requests for which responses have not been received.

Claim 16 (original): A model as claimed in claim 15, wherein the maximum number of requests which can be stored in the queue is definable.

Claim 17 (currently amended): A computer implemented model of a target to be used in designing an integrated circuit in which one or more initiators

are arranged to send packet-format requests to a target and the target is arranged to send packet-format responses to the requests via an interconnect, said model embodied as a plurality of parameters stored in a computer file, said model comprising:

a locking stage for causing a computer to permit ~~which permits~~ locked transactions to occur if required; and

a decode state for causing the computer to decode ~~which decodes~~ information stored in a first queue into an address for the response.

Claim 18 (previously presented): A model as claimed in claim 17, wherein said model comprises an access queue which stores information on the requests received by the target.

Claim 19 (previously presented): A model as claimed in claim 18, wherein a maximum number of outstanding requests which can be stored in said first queue is definable.

Claim 20 (original): A model as claimed in claim 17, wherein said queue is in the initiator.

Claim 21-24 (cancelled)

Claim 25 (currently amended): A computer implemented method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining whether the initiator or the interconnect is to be responsible for ordering packet-format responses to requests issued by said initiator;

defining whether a delay stage is required in said initiator; [[and]]

storing parameters in a computer file indicating results of the defining steps[[.]] ; and

processing the stored parameters to produce a description of the integrated circuit.

Claim 26 (new): The method of claim 1, wherein the produced description comprises a register to transfer level description of the integrated circuit, a functional description of the integrated circuit, or a performance description of the integrated circuit.

Claim 27 (new): The method of claim 26, wherein the processing is performed by a modeling program operating on a computer system and the description of the integrated circuit is output of the modeling program that comprises a computer net list.

Claim 28 (new): The method of claim 5, further comprising representing the defined number of routing resources, the defined arbitration method, and the defined association as parameters stored in a computer file for use in the processing step.

Claim 29 (new): The method of claim 25, wherein the produced description comprises a register to transfer level description of the integrated circuit, a functional description of the integrated circuit, or a performance description of the integrated circuit.